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EXAMINER	
SMITH, FRANCIS P	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,172	PARTRIDGE ET AL.	
	Examiner	Art Unit	
	FRANCIS P. SMITH	4151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

"Tetaethoxysilane" has been misspelled throughout the entire specification and should be spelled "Tetraethoxysilane".

"think layer 60" should be "thin layer 60" ([0069], line 5).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-11 and 41-51 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et al. (US 5,869,384).

Yu et al. teaches a method for forming a silicon oxide layer on a substrate. Regarding claims 1 and 41, a silicon oxide trench fill layer is formed through an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material at an ozone:TEOS volume ratio of 13:1, a reactor chamber pressure of about 450 torr, and a substrate temperature of 400°C, which is analogous to positioning a substrate in a deposition chamber (inherent) and oxidizing/decomposing a silicon precursor gas in a

deposition chamber at a first temperature to form a silicon oxide layer (col. 9, lines 46-55). Then, the substrate was annealed at a second temperature of 1100°C, which is higher than the first temperature (col. 10, lines 40-47).

As per claims 2 and 42, ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claims 3,8,43, and 48, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

Regarding claims 4,9,44, and 49, Yu teaches a second temperature (1100°C) that is approximate to the highest processing temperature (about 920°C) col. 10, lines 4-12; col. 10, lines 49-55.

As for claims 5,6,45, and 46, a silicon layer was formed on a substrate at a low pressure of 10 T (col. 9, lines 36-45)

As per claims 7 and 47, ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claims 10 and 50, Yu employs a tetraethoxysilane (TEOS) as a silicon precursor gas (col. 9, lines 46-51).

Regarding claims 11and 51, a silicon oxide layer formed through Yu's ozone assisted sub-atmospheric pressure chemical vapor deposition (SACVD) method yielded

comparatively little shrinkage upon thermal annealing within an oxygen containing atmosphere, thus providing thermally oxidized contiguous layers where there is limited stress formed therein (i.e. relieving compressive stress)(col. 11, lines 16-25).

3. Claims 31,37, and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Reichenbach et al. (US 2004/0065932).

Reichenbach teaches a method for producing a sensor with at least one micromechanical structure. For claim 31, Reichenbach teaches depositing a silicon-based, CVD oxide layer over at least a portion of the mechanical structure at a first temperature of about 200-300°C ([0044], lines 1-3 and 13-16). Reichenbach teaches annealing (i.e. heating) the sacrificial oxide layer at a second temperature higher than the first at 1000°C [0046, lines 7-11). A first encapsulation layer (i.e. deposition layer of polysilicon) is then deposited, which is analogous to depositing a first encapsulation layer over the sacrificial oxide layer ([0046], lines 1-3). The polysilicon layer (first encapsulation layer) contains small etch openings (i.e. at least one vent) to allow removal of at least a portion of the sacrificial oxide layer ([0048], lines 1-8). The sacrificial layer is removed (etched) to form a chamber, which is analogous to removing a portion of the sacrificial oxide layer. A second encapsulation layer (i.e. sealing layer) is deposited after the sacrificial layer etch and creates a hermetic seal ([0049], lines 1-3).

Regarding claims 37 and 38, the sacrificial oxide layer is etched via the trenches by and HF vapor etching process ([0043], lines 1-8; [0048], lines 1-8).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims12-15 and 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Xia et al. (US 6,602,806).

Yu teaches a method for forming a silicon oxide layer on a substrate with the said substrate having an N or P-doping. Yu, however is silent in respect to the silicon oxide layer containing a dopant.

Xia discloses a thermal CVD process for depositing a low dielectric constant carbon-doped silicon oxide film. Specifically, the method entails depositing a low dielectric constant film such as a carbon-doped silicon oxide layer deposited from a thermal CVD process (see abstract). Additionally, one or more dopants may be included with the organosilane and ozone during deposition of the low-k layer for both PMD and IMD applications. Phosphorus may be added using phosphine during the deposition described above to getter alkali metals (i.e. sodium), thereby reducing metal contamination of the deposited film. Boron may also be added using diborane. Alternatively, one or more dopants, such as phosphorus and/or boron, may be included in the process gas (col. 2, lines 66-67; col. 16, lines 58-68). Therefore, it would have been obvious to one skilled in the art at the time of the invention to utilize one or more dopants in the silicon oxide layer of Yu as taught by Xia to produce a film with a low dielectric constant for use in pre-metal and inter-metal dielectric layers to ultimately reduce the RC time delay of the interconnect metallization, to prevent cross-talk between the different levels of metallization, and to reduce device power consumption.

8. Claims 16-18,22-24,26, 29, and 30, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898).

Regarding claim 16, Yu et al. teaches a method for forming a silicon oxide layer

on a substrate. A silicon oxide trench fill layer is formed through an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source material at an ozone:TEOS volume ratio of 13:1, a reactor chamber pressure of about 450 torr, and a substrate temperature of 400°C (which is analogous to positioning a substrate in a deposition chamber (inherent) and oxidizing/decomposing a silicon precursor gas in a deposition chamber at a first temperature to form a silicon oxide layer) (col. 9, lines 46-55). Then, the substrate was annealed at a second temperature of 1100°C, which is higher than the first temperature (col. 10, lines 40-47). Yu, however, is silent with regard to forming a MEMS structure on a substrate.

Polson teaches a method of fabricating a MEMS device and teaches placing MEMS on semiconductor substrates (i.e. silicon wafers) (col. 1, lines 13-15). It would be obvious to one having ordinary skill in the art to add a MEMS device as taught by Polson to Yu's substrate in order to create micro electromechanical systems, such as high frequency circuits and MEMS accelerometers.

For claim 17, Yu teaches an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

As per claim 18, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

As for claims 22 and 26, Yu teaches a second temperature (1100°C) that is

approximate to the highest processing temperature (about 920°C) col. 10, lines 4-12; col. 10, lines 49-55.

Regarding claim 23, Yu discloses a silicon layer was formed on a substrate at a low pressure of 10 T (col. 9, lines 36-45).

For claim 24, Yu teaches ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method employed an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60).

For claim 29, Yu employs a tetraethoxysilane (TEOS) as a silicon precursor gas (col. 9, lines 46-51).

For claim 30, a silicon oxide layer formed through Yu's ozone assisted sub-atmospheric pressure chemical vapor deposition (SACVD) method yielded comparatively little shrinkage upon thermal annealing within an oxygen containing atmosphere, thus providing thermally oxidized contiguous layers where there is limited stress formed therein (col. 11, lines 16-25).

9. Claims 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898) as applied to claim 18 above, and further in view of Watanabe et al. (US 5,256,247).

Yu et al. as modified by Polson is silent with regard to etching the silicon oxide layer without producing an etch residue.

Watanabe teaches etching a chromium silicon dioxide layer of a resistor material

in an electronic integrated circuit without the formation of etch residue (col. 7, lines 44-50). Therefore, it would have been obvious to one skilled in the art at the time of the invention to adapt Yu's method as modified by Polson by incorporating Watanabe's etchant in order to prevent etch residue from hindering the performance of the integrated circuit.

Addressing claim 25, Yu discloses heating (annealing) the substrate in an oxygen-rich environment (col. 10, lines 49-55).

10. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Polson et al. (US 6,544,898), Watanabe et al. (US 5,256,247) as applied to claim 19 above, and further in view of Torek et al. (US 5,990,019).

Yu et al. as modified by Polson and Watanabe is silent with regard to etching the silicon oxide layer using a HF-vapor etch.

Torek et al. teaches a method of employing vapor phase etchants for etching oxides of silicon during the manufacture of a semiconductor devices that utilizes a gaseous mixture of HF and water as the etchant, which is analogous to a HF-vapor etch (col. 2, lines 46-54). Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate Torek's HF-vapor etch in Yu's method as modified by Polson and Watanabe in order to remove native oxides and other types of oxide contaminants during capacitor formation without excessively attacking the doped

silicon dioxide layer.

11. Claims 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US 5,869,384) in view of Watanabe et al. (US 5,256,247), Polson et al. (US 6,544,898), and Torek et al. (US 5,990,019) as applied to claim 21 above, and further in view of Chen et al. (US 5,904,570).

For claim 27, Watanabe discloses etching an oxide layer in two separate stages, which is analogous to applying a first and second etching process (col. 4, lines 4-10). However, Watanabe is silent regarding oxidizing the resulting residue.

Chen teaches a method for polymer removal after etching residue is exposed to an oxygen plasma, which is analogous to oxidizing etch residue (col. 2, lines 43-49). Therefore, it would be obvious to one skilled in the art at the time of the invention to adapt the method of Yu as modified by Watanabe, Polson, and Torek by further incorporating Chen's oxidizing plasma in order to effectively remove the etching residue to enhance subsequent manufacturing processes and ensure circuit functionality and reliability.

As per claim 28, Yu et al. as modified by Watanabe, Polson, and Torek is silent with regard to etching the silicon oxide layer using a HF-vapor etch.

Torek et al. teaches a method of employing vapor phase etchants for etching oxides of silicon during the manufacture of a semiconductor devices that utilizes a gaseous mixture of HF and water as the etchant, which is analogous to a HF-vapor etch (col. 2, lines 46-54). Therefore, it would have been obvious to one skilled in the art at

the time of the invention to incorporate Torek's HF-vapor etch in Yu's method in order to remove native oxides and other types of oxide contaminants during capacitor formation without excessively attacking the doped silicon dioxide layer.

12. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichenbach et al. (US 2004/0065932) in view of Yu et al. (US 5,869,384) and further in view of Ouellet (US 6,635,509).

For claim 32, Reichenbach teaches a method for producing a sensor with at least one micromechanical structure where the oxide layer (i.e. sacrificial oxide layer) is a CVD oxide ([0044], lines 1-3). However, Reichenbach is silent regarding depositing an oxide layer in an oxygen-rich environment.

Yu teaches a method for forming a silicon oxide layer on a substrate by an ozone assisted sub-atmospheric pressure thermal chemical vapor deposition method that employs an oxygen (ozone carrier gas) flow rate of about 5000 sccm, which is providing an oxygen rich environment in the deposition chamber during the oxidation of the silicon precursor gas (col. 9, lines 55-60). It would be obvious to one skilled in the art at the time of the invention to employ Yu's oxygen-rich environment to Reichenbach's method in order to provide a stable oxygen atmosphere inert to that particular layer.

For claim 33, Reichenbach as modified by Yu teaches a method for producing a sensor with at least one micromechanical structure, however, is silent regarding annealing the sacrificial oxide layer in an oxygen-rich environment.

Ouellet teaches a competitive, simple, single-substrate wafer-level packaging

technique capable of creating a vacuum-sealed protective cavity around moving or other particular components of a MEMS. Specifically, Ouellet teaches an annealing step performed in an oxygen-rich ambient (col. 10, lines 55-63). It would be obvious to one skilled in the art at the time of the invention to anneal the oxide layer of Reichenbach in an oxygen-rich environment as taught by Ouellet in order to provide a stable oxygen atmosphere inert to that particular layer.

13. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichenbach et al. (US 2004/0065932) in view of Warren (US 5,503,285).

For claim 34, Reichenbach teaches a method for producing a sensor with at least one micromechanical structure where the semiconductor material used as the second encapsulation layer to seal the chamber is silicon nitride. Reichenbach does not teach using polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, or gallium arsenide.

Warren discloses a method for forming an electrostatically force balance silicon accelerometer where amorphous silicon us used as a sealing layer (analogous to the second encapsulation layer) col. 9, lines 62-67; col. 10, lines 1-2. It would be obvious to one skilled in the art at the time of the invention to adapt Reichenbach's method by incorporating Warren's amorphous silicon in order to cover a larger area for use in large-area electronic applications.

For claim 35, Reichenbach teaches a first encapsulation layer (i.e. deposition layer of polysilicon) is then deposited, which is analogous to depositing a first

encapsulation layer over the sacrificial oxide layer ([0046], lines 1-3).

14. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reichenbach et al. (US 2004/0065932) in view of Prall et al. (US 5,637,518).

Reichenbach teaches a method for producing a sensor with at least one micromechanical structure that uses polycrystalline silicon (i.e. polysilicon) in the first encapsulation layer. However, Reichenbach is silent regarding the use of monocrystalline silicon as part of the encapsulation layer.

Prall discloses a method of making a field effect transistor relative to a monocrystalline silicon substrate and includes a gate encapsulated by a layer comprised of monocrystalline and polycrystalline portions (see abstract). Therefore, it would be obvious to one skilled in the art at the time of the invention to incorporate Prall's encapsulation layer in Reichenbach's method in order to obtain an enhanced encapsulation layer with better efficiency and stability.

15. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reichenbach et al. (US 2004/0065932) in view of Yu (US 5,869,384).

For claim 39 Reichenbach is silent regarding a specific silicon precursor gas.

Yu teaches a method for filling a trench within a substrate with a gap filling silicon oxide trench fill layer. Yu employs a tetraethoxysilane (TEOS) as a silicon precursor gas (col. 9, lines 46-51). Therefore, it would be obvious to one skilled in the art at the time of the invention to use Yu's TEOS as a silicon precursor gas in Reichenbach's method

in order to form the silicon oxide layer.

For claim 40, Reichenbach does not teach heating the substrate to ultimately relieve internal stress.

In Yu's method, a silicon oxide layer formed through Yu's ozone assisted sub-atmospheric pressure chemical vapor deposition (SACVD) method yielded comparatively little shrinkage upon thermal annealing within an oxygen containing atmosphere, thus providing thermally oxidized contiguous layers where there is limited stress formed therein (i.e. relieving compressive stress)(col. 11, lines 16-25). Therefore, it would be obvious to one skilled in the art at the time of the invention to adapt Reichenbach's method by incorporating Yu's stress relieving technique in order to prevent from future silicon oxide layer fracturing that would result in a defective device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANCIS P. SMITH whose telephone number is (571)270-3717. The examiner can normally be reached on Monday through Friday 7:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571)272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FPS

/Michael Kornakov/
Supervisory Patent Examiner, Art Unit 4151